

WHAT IS CLAIMED IS:

1. An edge deviation calculation method in which a desired pattern is compared with a finish pattern to be formed on a wafer, which is predicted from a design pattern, based on a calculation of a light beam intensity, and a deviation quantity of the finish pattern from the desired pattern at each of edges of the finish pattern and the desired pattern is calculated, the calculation method comprising:
 - 10 setting a reference light beam intensity for setting the desired pattern on a wafer;
 - setting an evaluation point for comparison of the finish pattern with the desired pattern;
 - calculating a light beam intensity at the evaluation point;
 - 15 calculating a differentiation value of the light beam intensity at the evaluation point;
 - calculating an intersection of the differentiation value with the reference light beam intensity; and
 - 20 calculating a difference between the intersection and the evaluation point,
 - wherein the difference is defined as an edge deviation quantity of the finish pattern from the desired pattern.
- 25 2. An edge deviation calculation method in which a desired pattern is compared with a finish pattern to be formed on a wafer, which is predicted from a design

pattern, based on a calculation of a light beam intensity, and a deviation quantity of the finish pattern from the desired pattern at each of edges of the finish pattern and the desired pattern is
5 calculated, the calculation method comprising:

setting a reference light beam intensity for
setting the desired pattern on a wafer;

setting an evaluation point for comparison of the
finish pattern with the desired pattern;

10 calculating a light beam intensity at the
evaluation point;

calculating a differentiation value of the light
beam intensity at the evaluation point; and

dividing a difference between the light beam
15 intensity at the evaluation point and the reference
light beam intensity by the differentiation value,

wherein a result of the division is defined as
an edge deviation quantity of the finish pattern from
the desired pattern.

20 3. The edge deviation calculation method
according to claim 1, wherein the design pattern is a
design pattern which specifies a complex transmission
rate distribution, and the calculating of the light
beam intensity at the evaluation point comprises:

25 calculating Foulrier transform of the complex
transmission rate distribution of the design pattern;

calculating a mutual transmission coefficient;

calculating a product of the mutual transmission coefficient with the complex transmission rate distribution and a value obtained as a result of the Foulrier transform of the complex transmission rate distribution; and

calculating reverse Foulrier transform of the product.

4. The edge deviation calculation method according to claim 2, wherein the design pattern is a design pattern which specifies a complex transmission rate distribution, and the calculating of the light beam intensity at the evaluation point comprises:

calculating Foulrier transform of the complex transmission rate distribution of the design pattern;

calculating a mutual transmission coefficient;

calculating a product of the mutual transmission coefficient with the complex transmission rate distribution and a value obtained as a result of the Foulrier transform of the complex transmission rate distribution; and

calculating reverse Foulrier transform of the product.

5. The edge deviation calculation method according to claim 1, wherein the calculating of the light beam intensity at the evaluation point is obtained by a polynomial of n-story (n is a natural number) differentiation of the light beam intensity at

the evaluation point.

6. The edge deviation calculation method according to claim 2, wherein the calculating of the light beam intensity at the evaluation point is
5 obtained by a polynomial of n-story (n is a natural number) differentiation of the light beam intensity at the evaluation point.

7. The edge deviation calculation method according to claim 5, wherein, when an n-story
10 differentiation of a light beam intensity in the vicinity of a position coordinate $x = a$ of the evaluation point is defined as $f(x)^{(n)}$ ($n = 1, 2, \dots$), and a coefficient is defined as C_m ($m = 0, 1, 2, \dots$), a polynomial of the n-story differentiation is provided
15 as the following polynomial:

$$f(x) = C_0 f(x=a) + C_1 f^{(1)}(x=a)(X-a) + \dots + C_{m-1} f^{(n-1)}(x=a)(X-a)^{n-1} + C_m f^{(n)}(x=a)(X-a)^n.$$

8. The edge deviation calculation method according to claim 6, wherein, when an n-story
20 differentiation of a light beam intensity in the vicinity of a position coordinate $x = a$ of the evaluation point is defined as $f(x)^{(n)}$ ($n = 1, 2, \dots$), and a coefficient is defined as C_m ($m = 0, 1, 2, \dots$), a polynomial of the n-story differentiation is provided
25 as the following polynomial:

$$f(x) = C_0 f(x=a) + C_1 f^{(1)}(x=a)(X-a) + \dots + C_{m-1} f^{(n-1)}(x=a)(X-a)^{n-1} + C_m f^{(n)}(x=a)(X-a)^n.$$

9. The edge deviation calculation method according to claim 5, wherein a polynomial of the n-story differentiation is provided as the following polynomial in which n-story differentiation of a light beam intensity in the vicinity of a position coordinate $x = a$ of the evaluation point is obtained by Taylor expansion when $x = a$:

$$f(x) = f(x = a) + f^{(1)}(x = a)(X - a)/1! + f^{(2)}(x = a)/2!(X - a)^2 + \dots + f^{(n)}(x = a)/n! \cdot (X - a)^n.$$

10. The edge deviation calculation method according to claim 6, wherein a polynomial of the n-story differentiation is provided as the following polynomial in which n-story differentiation of a light beam intensity in the vicinity of a position coordinate $x = a$ of the evaluation point is obtained by Taylor expansion when $x = a$:

$$f(x) = f(x = a) + f^{(1)}(x = a)(X - a)/1! + f^{(2)}(x = a)/2!(X - a)^2 + \dots + f^{(n)}(x = a)/n! \cdot (X - a)^n.$$

11. A edge deviation calculation method according claim 1, further comprising changing at least one of the reference light beam intensity and focus within each of determined ranges, and comparing the mask pattern with the finish pattern.

12. A edge deviation calculation method according claim 2, further comprising changing at least one of the reference light beam intensity and focus within each of determined ranges, and comparing the mask

pattern with the finish pattern.

13. A edge deviation calculation method according to claim 1, wherein the design pattern is a corrected pattern corrected to provide the desired pattern.

5 14. A edge deviation calculation method according to claim 2, wherein the design pattern is a corrected pattern corrected to provide the desired pattern.

15 15. An edge deviation quantity verification method in which a desired pattern is compared with a finish pattern to be formed on a wafer, which is predicted from a design pattern, based on a calculation of a light beam intensity, a deviation quantity of the finish pattern from the desired pattern at each of edges of the finish pattern and the desired pattern is calculated, and it is determined whether or not the design pattern is to be corrected based on a result of the calculation of the deviation quantity, the verification method comprising:

20 setting a reference light beam intensity for setting the desired pattern on a wafer;

 setting an evaluation point for comparison of the finish pattern with the desired pattern;

 calculating a light beam intensity at the evaluation point;

25 calculating a differentiation value of the light beam intensity at the evaluation point;

 calculating an intersection of the differentiation

value with the reference light beam intensity;

calculating a difference between the intersection
and the evaluation point, and define the calculated
difference as an edge deviation quantity of the finish
5 pattern from the desired pattern; and

verifying the edge deviation quantity,

wherein, in the case where the edge deviation
quantity exceeds an allowable range, the design pattern
is corrected based on the deviation quantity.

10 16. An edge deviation quantity verification method
in which a desired pattern is compared with a finish
pattern to be formed on a wafer, which is predicted
from a design pattern, based on a calculation of
a light beam intensity, a deviation quantity of the
15 finish pattern from the desired pattern at each of
edges of the finish pattern and the desired pattern is
calculated, and it is determined whether or not the
design pattern is to be corrected based on a result
of the calculation of the deviation quantity, the
20 verification method comprising:

setting a reference light beam intensity for
setting the desired pattern on a wafer;

setting an evaluation point for comparison of the
finish pattern with the desired pattern;

25 calculating a light beam intensity at the
evaluation point;

calculating a differentiation value of the light

beam intensity at the evaluation point;

dividing a difference between the light beam intensity at the evaluation point and the reference light beam intensity by the differentiation value, and

5 defining a result of the division as an edge deviation quantity; and

verifying the edge deviation quantity,

wherein, in the case where the edge deviation quantity exceeds an allowable range, the design pattern
10 is corrected based on the deviation quantity.

17. An edge deviation quantity verification program in which a desired pattern is compared with a finish pattern to be formed on a wafer, which is predicted from a design pattern, based on a calculation
15 of a light beam intensity, a deviation quantity of the finish pattern from the desired pattern at each of edges of the finish pattern and the desired pattern is calculated, and it is verified whether or not the design pattern is to be corrected based on a result
20 of the calculation of the deviation quantity, the verification program comprising:

setting a reference light beam intensity for
setting the desired pattern on a wafer;

25 setting an evaluation point for comparison of the finish pattern with the desired pattern;

calculating a light beam intensity at the evaluation point;

calculating a differentiation value of the light beam intensity at the evaluation point;

calculating an intersection of the differentiation value with the reference light beam intensity;

5 calculating a difference between the intersection and the evaluation point, and define the calculated difference as an edge deviation quantity of the finish pattern from the desired pattern; and

 verifying the edge deviation quantity,

10 wherein, in the case where the edge deviation quantity exceeds an allowable range as a result of the verification, the design pattern is corrected based on the deviation quantity.

 18. An edge deviation quantity verification
15 program in which a desired pattern is compared with a finish pattern to be formed on a wafer, which is predicted from a design pattern, based on a calculation of a light beam intensity, a deviation quantity of the finish pattern from the desired pattern at each of
20 edges of the finish pattern and the desired pattern is calculated, and it is verified whether or not the design pattern is to be corrected based on a result of the calculation of the deviation quantity, the verification program comprising:

25 setting a reference light beam intensity for setting the desired pattern on a wafer;

 setting an evaluation point for comparison of the

finish pattern with the desired pattern;

calculating a light beam intensity at the
evaluation point;

calculating a differentiation value of the light
5 beam intensity at the evaluation point;

dividing a difference between the light beam
intensity at the evaluation point and the reference
light beam intensity by the differentiation value, and
defining a result of the division as an edge deviation
10 quantity; and

verifying the edge deviation quantity,

wherein, in the case where the edge deviation
quantity exceeds an allowable range, the design pattern
is corrected based on the deviation quantity.

15 19. An edge position quantity verification system
having an input/output circuit, a storage, a computer,
a display and a controller, in which a desired pattern
is compared with a finish pattern to be formed on a
wafer, which is predicted from a design pattern, based
20 on a calculation of a light beam intensity, a deviation
quantity of the finish pattern from the desired pattern
at each of edges of the finish pattern and the desired
pattern is calculated, and it is verified whether or
not the design pattern is to be corrected based on
25 a result of the calculation of the deviation quantity,
the verification system comprising:

setting a reference light beam intensity for

setting the desired pattern on a wafer;

 setting an evaluation point for comparison of the
finish pattern with the desired pattern;

 calculating a light beam intensity at the
5 evaluation point;

 calculating a differentiation value of the light
beam intensity at the evaluation point;

 calculating an intersection of the differentiation
value with the reference light beam intensity;

10 calculating a difference between the intersection
and the evaluation point, and define the calculated
difference as an edge deviation quantity of the finish
pattern from the desired pattern; and

 verifying the edge deviation quantity,

15 wherein, in the case where the edge deviation
quantity exceeds an allowable range as a result of the
verification, the design pattern is corrected based on
the deviation quantity.

20 20. An edge position quantity verification system
having an input/output circuit, a storage, a computer,
a display and a controller, in which a desired pattern
is compared with a finish pattern to be formed on a
wafer, which is predicted from a design pattern, based
on a calculation of a light beam intensity, a deviation
25 quantity of the finish pattern from the desired pattern
at each of edges of the finish pattern and desired
pattern is calculated, and it is verified whether or

not the design pattern is to be corrected based on a result of the calculation of the deviation quantity, the verification system comprising:

5 setting a reference light beam intensity for
 setting the desired pattern on a wafer;
 setting an evaluation point for comparison of the
 finish pattern with the desired pattern;
 calculating a light beam intensity at the
 evaluation point;

10 calculating a differentiation value of the light
 beam intensity at the evaluation point;

 dividing a difference between the light beam
 intensity at the evaluation point and the reference
 light beam intensity by the differentiation value, and
15 defining a result of the division as an edge deviation
 quantity; and

 verifying the edge deviation quantity,
 wherein, in the case where the edge deviation
 quantity exceeds an allowable range, the design pattern
20 is corrected based on the deviation quantity.

21. A semiconductor device manufacturing method in
which a desired pattern is compared with a finish
pattern to be formed on a semiconductor wafer, which is
predicted from a design pattern, based on a calculation
25 of a light beam intensity, a deviation quantity of the
 finish pattern from the desired pattern at each of
 edges of the finish pattern and desired the pattern is

calculated, it is verified whether or not the design pattern is to be corrected based on a result of the calculation of the deviation quantity, and a semiconductor device is manufactured by using a mask having
5 the design pattern corrected based on the verification, the manufacturing method comprising:

setting a reference light beam intensity for setting the desired pattern on a wafer;

10 setting an evaluation point for comparison of the finish pattern with the desired pattern;

calculating a light beam intensity at the evaluation point;

calculating a differentiation value of the light beam intensity at the evaluation point;

15 calculating an intersection of the differentiation value with the reference light beam intensity;

calculating a difference between the intersection and the evaluation point, and define the calculated difference as an edge deviation quantity of the finish
20 pattern from the desired pattern;

verifying the edge deviation quantity;

correct the design pattern based on the deviation quantity, in the case where the edge deviation quantity exceeds an allowable range;

25 forming a mask having the design pattern corrected based on the deviation quantity; and

forming a pattern corresponding to the corrected

design pattern on a semiconductor wafer by using the mask to form a semiconductor device on the semiconductor wafer.

22. A semiconductor device manufacturing method
5 in which a desired pattern is compared with a finish pattern to be formed on a semiconductor wafer, which is predicted from a design pattern, based on a calculation of a light beam intensity, a deviation quantity of the finish pattern from the desired pattern at each of
10 edges of the finish pattern and the desired pattern is calculated, it is verified whether or not the design pattern is to be corrected based on a result of the calculation of the deviation quantity, and a semiconductor device is manufactured by using a mask having
15 the design pattern corrected based on the verification, the manufacturing method comprising:

setting a reference light beam intensity for
setting the desired pattern on a wafer;

20 setting an evaluation point for comparison of the finish pattern with the desired pattern;

calculating a light beam intensity at the
evaluation point;

calculating a differentiation value of the light
beam intensity at the evaluation point;

25 dividing a difference between the light beam intensity at the evaluation point and the reference light beam intensity by the differentiation value, and

defining a result of the division as an edge deviation quantity; and

verifying the edge deviation quantity,

5 correct the design pattern based on the deviation quantity, in the case where the edge deviation quantity exceeds an allowable range;

forming a mask having the design pattern corrected based on the deviation quantity; and

10 forming a pattern corresponding to the corrected design pattern on a semiconductor wafer by using the mask to form a semiconductor device on the semiconductor wafer.